What is claimed is:

1. An instruction buffer comprising:

a sequence of instructions arranged in an order determined beforehand; and

a first buffer including entries arranged in a preselected order for storing said sequence of instructions;

wherein any one of said sequence of instructions stored in any one of the entries designated by a low entry number is prior, in order, to another instruction stored in another entry designated by a high entry number.

2. The instruction buffer as claimed in claim 1, wherein the entries each show whether or not the instruction stored therein is ready to be issued.

3. The instruction buffer as claimed in claim 2, wherein the instruction is first issued from, among the entries whose instructions are ready to be issued, the entry having a lowest entry number.

4. The instruction buffer as claimed in claim 3, wherein the entries storing the instructions are lower in entry number than the entries storing no instructions.

5. The instruction buffer as claimed in claim 4, further comprising a second buffer including other entries for storing instructions, wherein the instruction stored in any one of said other entries earlier than the other

instructions is issued earlier than said other instructions.

6. A method of controlling a buffer queue, comprising the steps of:

generating a first group of instructions in an order determined beforehand;

generating a second group of instructions belonging to said first group of instructions and capable of being executed; and

executing one of said second group of instructions highest in order.

7. The method as claimed in claim 6, further comprising the steps of:

generating a third group of instructions included in said first group of instructions; and

generating a fourth group of instructions included in said first group of instructions and not dependent on said third group of instructions;

wherein when one of said fourth group of instructions highest in order does not belong to said second group of instructions, none of said fourth group of instructions is executed.

8. The method as claimed in claim 7, wherein one of preselected two instructions belonging to said third group or said fourth group is not executable until the other

instruction is executed.

9. The method as claimed in claim 8, wherein the instructions belonging to said third group are executed at the same time as the instructions belonging to said fourth group.

10. The method as claimed in claim 9, wherein the instructions belonging to said third group and the instructions belonging to said fourth group are operation instructions and memory access instructions, respectively.